Complexity Analysis of an 8 point FFT Processor for different Butterfly Structures

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Abstract— **In general, Fast Fourier Transform (FFT) hardware unit has more computational elements, hence always consumes high power compared to any other computational counterparts. So, optimization of FFT architecture is always a challenge because of its complex structure. In this paper, we present the analysis of computational complexity of various FFT algorithms and the high performance Single-path Delay Feedback (SDF) architecture. The analysis has been done on 8 point FFT processor, designed and synthesized using Xilinx ISE tools.**

Keywords-Single-path Delay Feedback; Architecture; Algorithms; Synthesis

I. INTRODUCTION

Many communication and signal processing applications have FFT as the most power consuming block. This is because of its excessive computational complexity. The complexity of DSP algorithms is typically measured by the number of multiplications required [1]. There are many algorithms proposed in the literature to reduce the number of computations, in which some of them are not suitable for hardware implementation due to their structural irregularity [2]. Various architectures for hardware friendly algorithms are proposed and different modifications are addressed by the researchers for the reduced computational complexity and hence less power consumption.

In this work, an 8 point FFT processor is designed using VHDL for radix-2, radix-8 and radix-2^3 butterfly structures as shown in Figures 1, 2 and 3. As presented in [3], there are two designs for radix-2^3 butterfly structure, design-I is with multipliers for the two non trivial complex multiplications and design-II is with shift add structure as shown in Figure 4 to implement the multiplications with complex numbers $\sqrt{2}/2$ (1 $\pm$ j) [5], which are nothing but the twiddle factors for the non trivial multiplications.

II. PROCESSOR DESIGN FOR 8 POINT FFT

The block diagram for an 8 point FFT processor is shown in Figure 5, in which serial input data samples are first converted into parallel using serial to parallel conversion block and then fed to the 8 point butterfly structure for FFT computation and the resultant output samples are then converted into serial using parallel to serial conversion block. The 8 point butterfly structure is replaced by different structures shown in section

to implement different designs. Functional verification is done using Xilinx ISIM simulator and the simulation results for all the processor designs are same as shown in Figure 6.

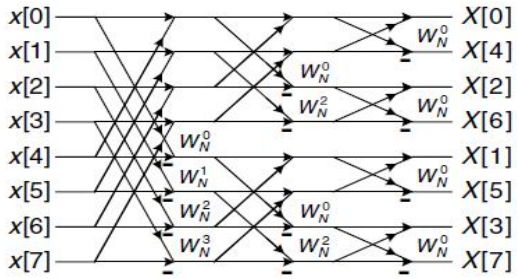

Figure 1. Butterfly structure for 8 point radix-2 FFT

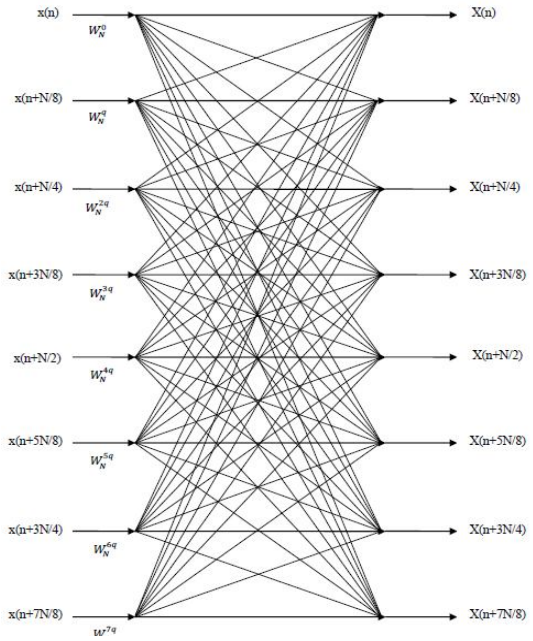

Figure 2. Butterfly structure for radix-8 FFT

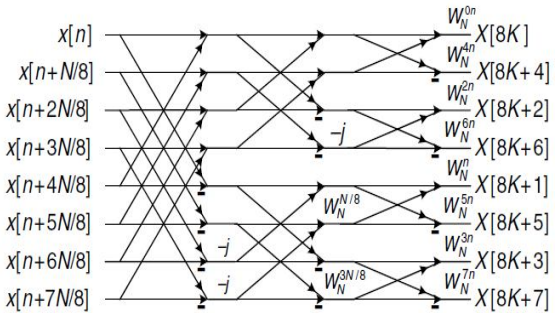

Figure 3. Butterfly structure for radix-2^3 FFT

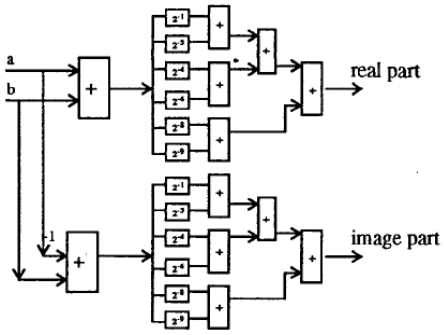

Figure 4. Structure for multiplication of (a + jb) with the complex number $\sqrt{2}/2\ (1 \pm j)$

These designs are synthesized using Xilinx ISE synthesis tool. The RTL schematics are shown in Figure 7, by which it is easily observed that in radix-8 FFT processor, though the multiplications are less, routing becomes tedious due to huge number of adders.

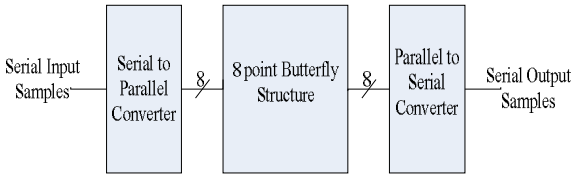

Figure 5. Block diagram of an 8 point FFT processor

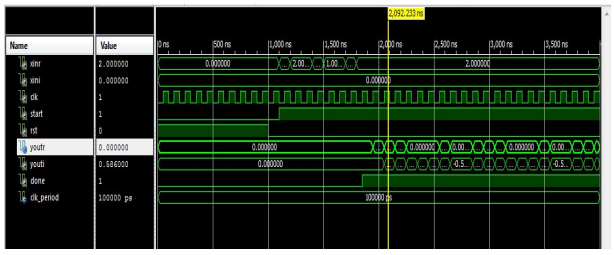

Figure 6. Simulation results of 8 point FFT

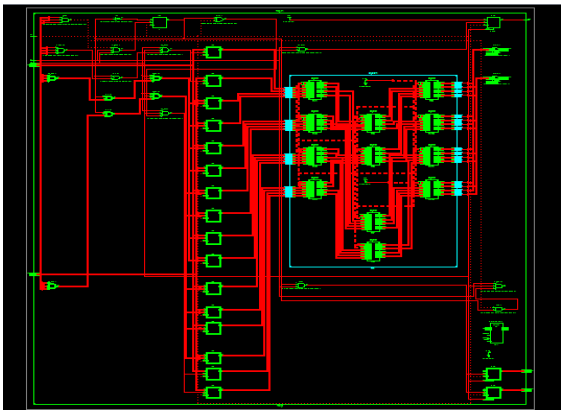

Figure 7(a). RTL schematic for radix-2 FFT

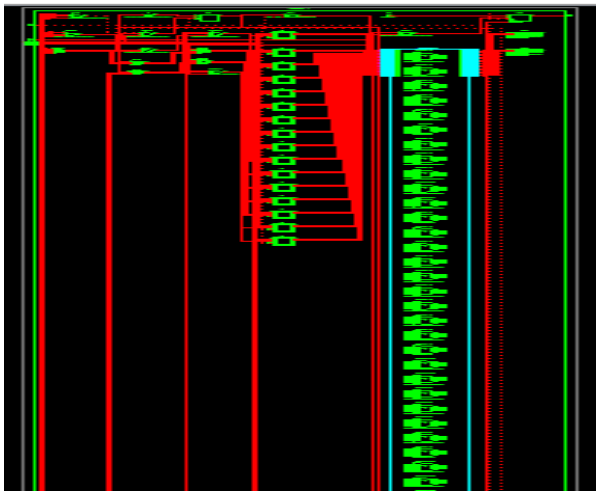

Figure 7(b). RTL schematic for radix-8 FFT

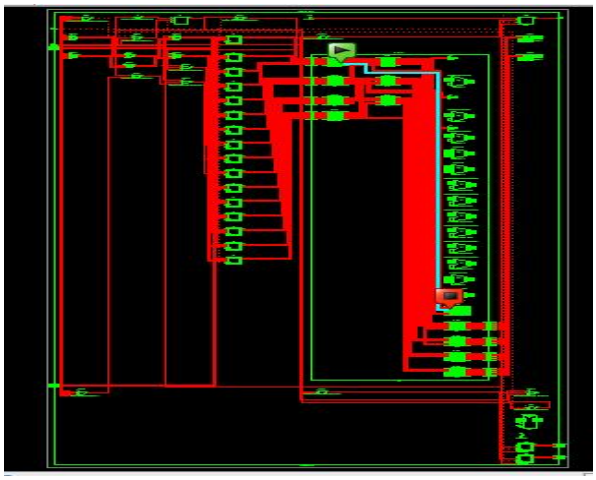

Figure 7(c). RTL schematic for radix-2^3 FFT (Design-I)

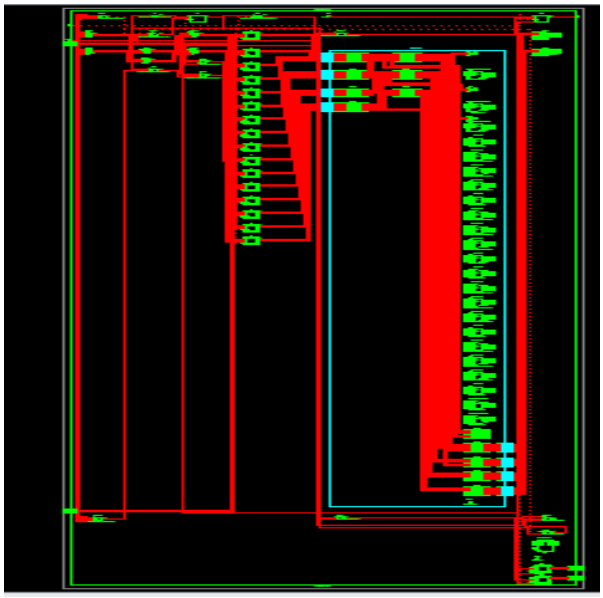

Figure 7(d). RTL Schematic for radix-2^3 FFT (Design-II)

A radix-2 pipelined Single-path Delay Feedback (SDF) architecture [4] for an 8 point FFT shown in Figure 8 is also designed and synthesized. In which the serial input samples are taken in normal order by the Processing Element (PE) (Figure 9) and selectively sent to the Delay Unit (DU) to perform butterfly operation between the respective samples according to the structure. The PE consists of multiplexers, de-multiplexers and a Butterfly unit, which is a simple structure with 2 adders and 2 subtractors as shown in Figure 10.

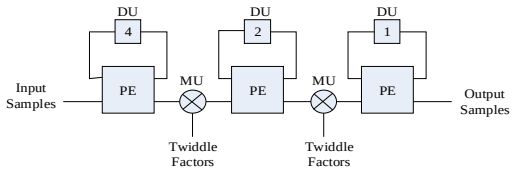

Figure 8. An 8 point radix-2 pipelined SDF FFT architecture

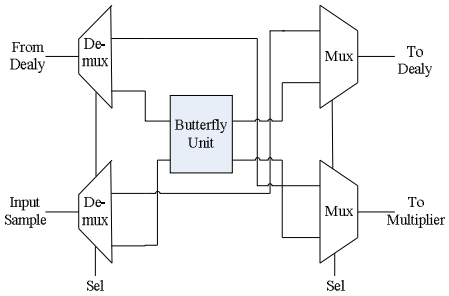

Figure 9. Processing Element (PE) of figure 8.

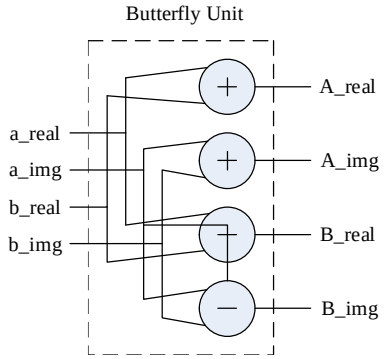

Figure 10. Butterfly unit used in PE

Once the butterfly operation is completed at each stage except the last stage, the processed samples are sent to Multiplier Unit (MU) (Figure 11), where the samples are multiplied with twiddle factors selectively. The output samples from the last stage are in bit reversed order. The RTL schematic for this design is shown in Figure 12. The Processor has a simple control circuitry to generate select signals for the multiplexers and de-multiplexers used in the PE and MU.

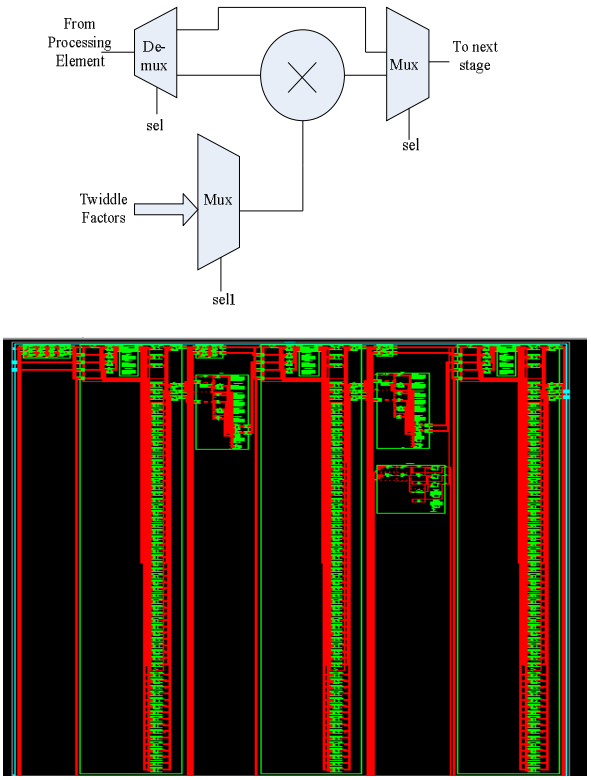

Figure 12. RTL schematic of proposed SDF architecture

III. RESULTS AND DISCUSSION

The proposed 8 point FFT processor is implemented in Xilinx Vertex-5 FPGA to observe the utilization of resources for each of the processor designs with different butterfly structures. Comparison of computational elements and other parameters between all the above designs is presented in Table I. As shown in the Table1, the radix-2 SDF structure gives the highest performance compared to the other designs with less resource utilization. This is due to the pipelined structure for improving the throughput. Among the other designs, radix-2^3 designs are economical and proved to be faster. In radix-8 design, due to large number of multiple input adders/subtractors, the interconnection structure becomes complex and hence causes more delay.

Table I. COMPARISON OF COMPUTATIONAL COMPLEXITY AND OTHER PARAMETERS

Algorithm	radix-2	radix-8	radix-2^3 design-I	radix-2^3 design-II	radix-2 SDF
No. of Multipliers	48	30	06	-	08
No. of 16 bit adders/subtractors	48	14	51	71	12
No. of 32 bit adders/subtractors	24	116	04	-	04
No. of Slices	762	1703	658	722	412
No. of Flip flops	293	293	293	293	557
No. of LUTs	1229	3328	1027	1082	590
Frequency(MHz)	67.088	**58.648**	86.338	109.719	**187.573**

IV. CONCLUSIONS AND FUTURE SCOPE

FFT processors are computationally intensive structures. The complexity is analyzed when different algorithms are used to implement an 8 point FFT. Besides different algorithms, the computational complexity of pipelined SDF architecture is also analyzed and compared. Results show that performance of FFT processor can be improved if pipelined structure is used instead of direct implementation of the butterfly structures. In future, higher point FFT processors can be used for analysis of different algorithms with pipelined structures.

REFERENCES

[1] William G. Bliss and Archie W. Julien, "Efficient and Reliable VLSI Algorithms and Architectures for the Discrete Fourier Transform", CH2847-2/90/0000-0901, IEEE, 1990.

[2] P. Duhamel and M. Vetterli "Fast Fourier transforms: a tutorial review and a state of the art", Signal Process.vol. 19, no. 4, pp. 259-299, 1990.

[3] Anwar Bhasha Pattan and Dr. M. Madhavi Latha "FPGA Implementation of an efficient radix-2^3 FFT Algorithm", in Proceedings of the National Conference on Emerging Trends in Information, Digital & Embedded Systems, NC'e-TIDES -15, 28th February 2015.

[4] S. He and M. Torkelson, "Designing pipeline FFT processor for OFDM (de)modulation", in Proc. of IEEE URSI International Symposium on Signals, Systems, and Electronics, Sep. 1998, pp. 257–262.